Growth of self-assembled nanostructures by molecular beam epitaxy

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A compact, custom-made molecular beam epitaxy (MBE) system has been installed and a commercial ultrahigh vacuum scanning tunnelling microscope (STM) has been coupled to the MBE chamber. Examples of growth of self-assembled nanostructures by MBE using this system and characterizations using reflection high energy electron diffraction, STM and high resolution transmission electron microscopy are presented.

NANOSCIENCE and nanotechnology have been attracting attention worldwide and they constitute an active, frontier area of research. Research in this area has not only stimulated the exploration of new phenomena, but is also leading to a technological revolution. For electronic devices, this research promises to extend device physics to full two- or three-dimensional confinement (quantum wires and dots). Multidimensional confinement in these low-dimensional structures has long been predicted to alter significantly the transport and optical properties, compared to bulk or planar heterostructures. More recently, the effect of charge quantization on transport in small semiconductor quantum dots has stimulated much research in single-electron devices, in which the transfer of a single electron is sufficient to control the device. The most important factor driving active research in quantum effect is the rapidly expanding semiconductor band-gap-engineering capability provided by modern epitaxy, such as molecular beam epitaxy (MBE) and metallorganic chemical vapour deposition (MOCVD).

MBE is a versatile technique for growing thin epitaxial structures made of metals, semiconductors and insulators. It is a vacuum deposition technique carried out in an ultrahigh vacuum (UHV) environment. What distinguishes MBE from earlier vacuum deposition techniques is its significantly more precise control of the beam fluxes and growth conditions. MBE growth is carried out under conditions far from thermodynamic equilibrium and is governed mainly by the kinetics of the surface processes occurring when the impinging beams interact with the outermost atomic layers of the substrate crystal. MBE has a unique advantage over all other epitaxial growth techniques. The growth being performed under UHV conditions may be controlled in situ by surface-sensitive diagnostic methods like reflection high energy electron diffraction (RHEED), Auger electron spectroscopy (AES) and ellipsometry. These powerful facilities for control and analysis enable the fabrication of sophisticated device structures using MBE.

Epitaxial growth is governed by some broad principles. In the case of heteroepitaxial growth there are three different growth modes: (a) Frank–van der Merwe (FM) or layer-by-layer growth, (b) Volmer–Weber (VW) or island growth and (c) Stranski–Krstanov (SK) or layer-plus-island growth. Which growth mode will be adopted in a given system depends on the surface free energy of the substrate, \( \sigma_s \), that of the film, \( \sigma_f \) and the interfacial energy \( \sigma_i \). Layer-by-layer growth mode occurs when \( \Delta \sigma = \sigma_f + \sigma_i - \sigma_s \leq 0 \). The condition of FM mode growth is rigorously fulfilled only for homoepitaxy (same film material as that of the substrate), where \( \sigma_f = \sigma_s \) and \( \sigma_i = 0 \). If the FM mode growth condition is not fulfilled, then three-dimensional crystals form immediately on the substrate (VW mode). For a system with \( \Delta \sigma \leq 0 \) but with a large lattice mismatch between the substrate and the film, initial growth is layer-by-layer. However, the film is strained. As the film grows in thickness, it stores an increasingly large strain energy. This strained epilayer system can lower its total energy by forming isolated thick islands in which the strain is relaxed by interfacial misfit dislocations, leading to SK growth in these strained systems.

SK growth mode occurs when there is a lattice mismatch between the substrate and the epilayer, causing the epilayer to be strained. Growth of dot-like self-assembled islands is a consequence of this. Wire-like islands can grow from dot-like islands via a shape transition which helps strain relaxation. This shape transition has been predicted and observed. The dot islands grow in a shape following the symmetry of the substrate. For example, equilateral triangular and square islands grow on a substrate of threefold and fourfold symmetry respectively. On a substrate with twofold symmetry, elongated island growth appears to be preferable.

For nanostructural fabrication, usually a thin epilayer is grown on a substrate. This two-dimensional (2D) layer is used to fabricate lower dimensional structures like wires (1D) or dots (0D) by lithographic techniques. However, structures smaller than the limits of conventional lithography techniques can only be obtained by self-

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assembled growth utilizing the principles of SK or VW growth. Due to their small size, these islands can exhibit unusual quantum confinement effects, which make them useful in electrical devices as single electron transistors and optical devices\textsuperscript{10}. For appropriate growth conditions, self-assembled epitaxial islands can be grown in reasonably well-controlled sizes\textsuperscript{11,12}. A narrow size distribution is essential for most optoelectronic applications. The ability to grow such size-controlled islands is an attractive feature of self-assembly, although the positions of individual islands cannot be determined precisely. Since precise placement of islands is not required for many devices, self-assembly is an attractive route for the fabrication of devices based on nanostructures.

**Ge growth on silicon**

We concentrate on the growth of Ge on silicon. More than 90% of all semiconductor devices are based on silicon. Ge/Si heteroepitaxial layers can be applied for new device concepts\textsuperscript{13,14}. First industrial applications of Ge/Si heteroepitaxial layers are heterobipolar transistors with an epitaxially grown Ge/Si basis\textsuperscript{15,16}. An important aspect is that the Ge/Si system is compatible with the standard CMOS technology used for the production of most semiconductor devices. Application of Ge/Si may be found in silicon-based optoelectronics in future. Due to the indirect band gap, Si devices are not well suited for optoelectronic applications. New devices employing Ge/Si epitaxial layers are expected to overcome this restriction\textsuperscript{15–17}. For example, Ge islands embedded in Si layers can be used for light emission. Electron–hole pairs are captured in Ge islands, where they recombine by light emission. For these kinds of applications, a dense array of small islands with a narrow size distribution is desirable. To achieve confinement effects at room temperature, the necessary island size is only a few nanometers. This is below the limits of conventional lithography. An alternative way to achieve this is the spontaneous self-assembly of 3D islands during the epitaxial growth of Ge on Si.

Growth of Ge on Si is a classic case of SK growth, where uniform layer-by-layer growth up to \( \sim 3 \) monolayers [1 monolayer (ML) is equivalent to \( 6.78 \times 10^{14} \) atoms/cm\(^2\) on a Si(100) surface and \( 7.8 \times 10^{14} \) atoms/cm\(^2\) on a Si(111) surface] is followed by island growth. Surface free energy of Ge is lower than that of Si. Hence Ge wets the Si surface – a condition for layer-by-layer growth. Both Ge and Si have diamond structure, but different sizes of the unit cell (lattice constant: \( a_{\text{Ge}} = 0.5657 \) nm, \( a_{\text{Si}} = 0.5431 \) nm). Due to 4.2% lattice mismatch between Ge and Si, a pseudomorphic Ge film grows with a strain. As the strain energy builds up, the competition between the surface energy and the strain energy eventually causes the film to undergo a 3D island growth at coverages beyond 3 ML\textsuperscript{18}. Three-dimensional island formation leads to a partial relaxation of strain. During growth, islands undergo a rich sequence of shape changes. On a Si(100) surface, initially they are square or rectangular shaped. They are termed as hut clusters\textsuperscript{19}. There are also other shapes like pyramid and dome\textsuperscript{20}. All these islands can be dislocation-free or coherent\textsuperscript{15}. Large islands usually contain misfit dislocations, the presence of which reduces the strain energy. The islands self-assembled via the SK growth mode are, in general, of nanometric dimension.

Before we discuss further the epitaxial growth of Ge, we discuss some other cases of self-assembled nanostructural growth of Ge. These could be obtained under high vacuum deposition on passivated surfaces. (Under high vacuum condition, even an atomically clean Si surface would get oxidized fast. However, it is possible to passivate some dangling bonds on the surface against oxidation by adsorbing monovalent atoms, such as halogens. This has been shown experimentally\textsuperscript{21} as well as theoretically\textsuperscript{22}. Such passivated Si surfaces have already been used for epitaxial growth on them\textsuperscript{23–25}). Self-assembled Ge nanolayers are also formed in Ge deposition on passivated Si substrates. Here, nanodots are formed on the surface of the deposited Ge layer by surface diffusion in a layer-to-island mass transport process\textsuperscript{23,24}. The surface diffusion activation energy was determined by X-ray reflectivity measurements\textsuperscript{25}. A small diffusion activation energy of 0.45 eV indicates that there is considerable surface diffusion of Ge even at room temperature. This information was utilized in the deposition of Ge on a polymer-coated Si surface to grow Ge nanodot and nanowire structures\textsuperscript{26–28}. In these cases the growth is governed mainly by the surface-free energies, whereas for epitaxial growth, in addition, the strain energy also plays a dominant role.

Very early stages (\( \sim 0.1--0.5 \) ML) of epitaxial growth of Ge on Si was investigated by Dev et al.\textsuperscript{26,27}. Eaglesham and Cerullo\textsuperscript{18} obtained self-assembled nanolayers of Ge on Si for depositions exceeding \( \sim 3 \) MLs. Since then, there have been many studies of Ge nanolayer growth using several epitaxial growth techniques. A recent review by Voigtländer\textsuperscript{29} discusses Ge epitaxial growth on Si. In the present article, on the one hand we report on the MBE growth of Ge on Si, because of a strong interest in this problem and on the other, to test the performance of our MBE system.

**Experimental**

First, we describe the equipment used for the growth and characterizations of self-assembled epitaxial nanolayers: A custom-made, compact MBE system along with the capability to transfer the MBE-grown samples to a UHV transfer chamber/suitcase as well as to a commercial UHV STM, designed by us in collaboration with and assembled by Omicron Vacuumphysik GmbH, has been installed in our laboratory. A UHV variable temperature scanning tunnelling microscope (VTSTM from Omicron) has been...
coupled with the MBE system at a later date. This system is shown in Figure 1. The UHV sample transfer chamber/suitcase has not yet been fabricated. (This transfer chamber can be a small UHV chamber into which the sample can be transferred. Then, this chamber along with its battery-operated UHV pump can be detached from the system and carried to an X-ray set-up for directly mounting on a goniometer for an X-ray scattering measurement. The important part of this chamber would be made of Be, so that X-rays can enter and exit through Be with practically no loss. Such a chamber is useful for synchrotron radiation-based experiments.) With the system shown in Figure 1, it is possible to grow and characterize thin epitaxial layers of metals and semiconductors on atomically clean surfaces of single crystal substrates. The MBE system has three Knudsen cells, a low-power electron beam evaporator, a quartz microbalance (QM) and a residual gas analyser (RGA). There is also an RHEED equipment fitted to the MBE unit for monitoring surface reconstruction and growth. For sample cleaning, it has direct heating as well as Ar ion sputtering facilities. The sample manipulator has a Z-translation (vertical) and the azimuthal angle can be varied over 360°. It also has a resistive heating facility so that the substrate temperature can be raised up to 900°C by resistive heating. Epitaxial growth of different materials is controlled by the substrate temperature and the rate of deposition. Out of the three Knudsen cells, one is capable of reaching 1400°C, the other two cells can reach 1700°C. The electron beam evaporator is used for deposition of silicon. With the option of three Knudsen cells and the electron beam evaporator, epitaxial multilayers can be grown. A load-lock chamber is attached with the main MBE chamber for initial sample mounting. A mounted sample in the load-lock chamber is transferred to the MBE chamber using a sample transfer mechanism on a magnetically coupled transfer rod. Using another transfer rod, the sample can be transferred to the VSTM stage for scanning tunneling microscopy (STM) studies without disturbing the UHV condition. The temperature range achievable in the VSTM is 25–1500 K. The best base pressure achieved in the MBE chamber is \(3 \times 10^{-11}\) mbar and that in the VSTM chamber is \(2 \times 10^{-10}\) mbar.

Recently, a 200 keV (JEOL 2010) high resolution transmission electron microscope (HRTEM) with pointto-point resolution of 0.19 nm and lattice resolution of 0.14 nm has been installed. A camera consisting of a yttrium–aluminium–garnet (YAG) scintillator that is fibre-optically coupled to an image intensifier, connected to a high-resolution television tube camera, provides a total magnification of 30 million (microscope magnification: \(1.5 \times 10^6\) and the camera magnification: 20). This imaging system outputs a video stream that is acquired in a computer with a frame-grabber. An option of using the films is also available. Sample preparation is an important aspect of the electron microscopy studies. To facilitate the sample preparation, an ultrasonic disc-cutter, a dimpler, a precision ion-polishing system (all from GATAN, USA), a grinder/polisher unit and a wire saw (Southbay Technology, USA) are available.

MBE growth and characterization by RHEED, STM and transmission electron microscopy (TEM) are performed in the following sequence. A Si(100) sample was cleaned, removing the native oxide by direct current heating at ~1250°C. On this surface RHEED measurements were made to obtain the characteristic (2 \(\times\) 1) reconstruction of the clean Si(100) surface. A thin (1.2 nm) Ge epilayer was grown by evaporating Ge from a Knudsen cell (Al\(_2\)O\(_3\) crucible) at a deposition rate of 0.05 nm/min with the substrate kept at 550°C. Layer thickness was directly measured during deposition by the quartz microbalance. The thickness was calibrated by post-deposition measurement using Rutherford backscattering spectrometry (RBS). Base pressure in the MBE chamber was \(1.0 \times 10^{-10}\) mbar. During growth, the pressure increased to \(8.5 \times 10^{-10}\) mbar. During deposition, RHEED measurements were also made. After deposition had been completed, the sample was transferred to the STM chamber. During STM measurement on the sample, the STM chamber pressure was \(2.5 \times 10^{-10}\) mbar. Having completed the STM measurements, the sample was taken out of the vacuum chamber for TEM measurements. Plan view and cross-sectional TEM studies on identically prepared Ge/Si samples were carried out \textit{ex situ}. For TEM studies, samples were prepared by mechanical polishing, dimple grinding and ion milling.

**Results and discussion**

\textbf{Clean surfaces of silicon}

It is extremely important to prepare an atomically clean surface of the substrate on which an epilayer is to be
grown. Common impurities like O and C on the surface should be brought down below the detection limit. This is usually checked by AES. However, RHEED can be used to detect characteristic diffraction patterns of clean surfaces and ensure that the substrate surface is clean before the deposition begins. The sample is degassed at 600°C for about 12 h in the MBE chamber. Following this, it is flashed at 1250°C for about 2–3 min by direct heating. In this process the native oxide on the Si surface desorbs and a clean silicon surface is produced. During this heating, the pressure in the chamber should not increase above $1 \times 10^{-9}$ mbar. The other way of preparing clean surfaces is Ar ion sputtering followed by annealing to have a clean, ordered surface. Clean silicon surfaces are reconstructed. Surface reconstruction is the rearrangement of the surface atoms due to the termination of the bulk structure at the solid–vacuum interface. The reconstruction of Si(111) and Si(100) surfaces has been observed by RHEED and STM. Si(111) surface shows a $(7 \times 7)$ reconstruction, whereas a Si(100) surface shows a $(2 \times 1)$ reconstruction. These are the characteristic signatures of clean Si(111) and Si(100) surfaces. Decades of research has led to an understanding of these surfaces. While RHEED shows the reconstruction in the reciprocal space, STM shows them in the real space. STM images of Si(111) and Si(100) surfaces are shown in Figures 2 and 3 respectively. In Figure 2 a, five unit cells on the $(7 \times 7)$ reconstructed surface are marked. The basis vectors $(a_i)$ of this unit cell are 2.695 nm, whereas on an ideal (unreconstructed) Si(111) surface the basis vectors $(a)$ would be 0.385 nm ($a = 7a$). The $(7 \times 7)$ reconstruction of the Si(111) surface is an old problem (1960s). It took over two decades to solve this structure. The accepted structural model of the Si(111) $(7 \times 7)$ surface is called dimer–adatom–stacking fault (DAS) model. In this model, each $(7 \times 7)$ unit cell contains Si–Si dimers along the unit cell edges, 12 adatoms per unit cell and stacking faults under one half of the unit cell. Twelve adatoms in a unit cell are clearly seen in Figure 2a. When the tunnelling condition is changed by reversing the STM bias voltage, the image shown in Figure 2b is obtained, where two unit cells are marked. Different structures of the two halves (faulted and unfaulted) of the unit cell give rise to different electronic structures in the two halves of the unit cell. This is reflected in the difference in STM images from the two halves in Figure 2b. In the unfaulted half, even the atoms from one layer below the adatoms are seen to contribute to the image. In fact, surface electronic states (both filled and empty) over a $(7 \times 7)$ unit cell have been identified with atomic resolution by measuring tunnelling current variation with applied bias.

Si(100) surfaces show a $(2 \times 1)$ reconstruction. On an ideal Si(100) $(1 \times 1)$ surface, the unit cell is a square $(a \times a)$. The $(2 \times 1)$ unit cell is rectangular $(2a \times a)$. Si–Si dimer rows are formed on the $(2 \times 1)$ reconstructed surface; these are seen in Figure 3a with the inset showing a magnified image. The surface is not smooth over large length scales. There are terraces and monatomic steps. The height difference between successive terraces $(T_1, T_2, T_3, T_4)$ is 0.136 nm. Meandering surface steps (one shown

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**Figure 2.** STM images of a Si(111) $(7 \times 7)$ surface at different bias voltages. **a.** Sample bias: +1.82 V, tunnelling current: 0.20 nA. Five surface unit cells are marked – one of them has a missing adatom; **b.** Sample bias: –1.82 V, tunnelling current: 0.16 nA. Two unit cells are marked. One half of the unit cell appears different from the other. One half of the unit cell has stacking fault and other half has normal stacking. Under this sample bias condition, the difference in tunnelling behaviour from the two halves leads to the difference in the STM images of the two halves.
as S) are also seen in the STM image. How the dimer rows are formed is illustrated in Figure 3 b. The dangling-bond orientation is rotated by 90° on successive terraces (a consequence of the diamond structure). This is responsible for the alternate directions of the dimer rows on successive terraces. Both Figures 2 and 3 a show some missing atoms (defects).

These are features of atomically clean Si(111) and Si (100) surfaces. For epitaxial growth on clean surfaces by MBE, one has to obtain these characteristic features of a clean, ordered surface before starting the deposition process.

Ge deposition and nanoisland formation

As mentioned earlier, one special advantage of MBE growth is the possibility of in situ monitoring and control of growth by techniques like RHEED, AES and/or ellipsometry. We have performed RHEED studies for this purpose. RHEED pattern from a Si(100) surface, measured with a 15 keV electron beam, is shown in Figure 4 a. This shows a (2 × 1) surface reconstruction, which is the signature of a clean Si(100) surface. Figure 4 b and c represents the changes in the RHEED pattern during MBE growth of Ge on the Si(100) surface. When Ge starts growing on the (2 × 1) surface, the reconstruction changes to (1 × 1). For a two-dimensional crystal the reciprocal lattice points are actually lattice rods. The Ewald’s sphere for the 15 keV electron beam impinging on the surface at a grazing incidence (3°) cut the surface reciprocal rods in elongated lines. This produces streak-shaped diffraction spots as seen in Figure 4 a for (2 × 1) reconstructed Si surface and in Figure 4 b for a 2D Ge layer. This is the signature of growth as layer-by-layer. As growth continues, islands start growing beyond a deposition of 3–4 MLs (0.4–0.5 nm) and 3D island growth becomes dominant. Hence the streaked RHEED spots evolve into points, as expected for 3D growth. This is seen in the RHEED pattern in Figure 4 c, when 1.2 nm Ge has been deposited. The change in RHEED pattern from Figure 4 b to c indicates a 2D to 3D transition, as expected in the SK growth.

Having stopped the growth, the Ge/Si(100) sample has been transferred to the STM chamber for further studies. This transfer is done without disturbing the UHV condition of the system. In Figure 5 an STM image from this sample is shown. Nanometer-scale Ge islands are now clearly seen in the real space. The islands are of square and rectangular shapes (although they have some rounded facets). Square-island growth is expected from the fourfold symmetry of the Si(100) surface. However, rectangular shape is also possible through a shape transition. These large islands have flat top. Smaller islands can have hut shapes. With increasing coverage, one also gets pyramid and dome-shaped islands. It is possible to get coherent islands up to a maximum size, beyond which islands grow with dislocations at the interface. However, whether the islands have dislocations or not cannot be observed in the STM images. High resolution cross sectional transmission electron microscopy (XTEM) is more suitable for this purpose.

The planar and the cross-sectional TEM specimens of Ge/Si samples were prepared for two different thicknesses (1.2 and 1.5 nm) of Ge on Si(100) substrates. The plan view image shown in Figure 6 a corresponds to a Ge thickness of 1.5 nm. Some moiré-fringes are seen on the islands. A detailed study of the spacing, variation of spa-
cing within an island and discontinuity of the moiré fringes can give evidence for the presence of misfit dislocations, nonuniform distribution of strain in an island and dislocation threading to the island surface respectively \(^{31-33}\). Also, we have observed (data not shown) evidence for other types of defect such as twins in Ge islands grown on a Si(110) substrate. Figure 6b shows cross-sectional image of a Ge island on Si and the Ge/Si interface. Images of many such islands have been used to study the Ge island height and shape variation as a function of substrate orientation and other growth parameters (Spatapi, B. et al., unpublished data). In order to show the high-resolution capability, a lattice resolution image from a planar Si(110) sample is shown in Figure 6c. Figure 6d shows a lattice image of a Ge island, where the outer boundary of the island is seen. Such images across the Ge/Si interface are used to identify misfit dislocations and other defects \(^{31-33}\).

Presence of dislocations reduces the strain in the islands. For Ge/Si(100) samples grown at various substrate temperatures in the range 500–800°C, we have carried out strain measurements by X-ray diffraction. Growth at higher substrate temperatures is intended to cause alloying and formation of Ge\(_{1-x}\)Si\(_x\) structures. For such alloy systems, energy band gap can be tuned \(^{3}\) to values between those of Ge and Si by controlling the value of \(x\). This offers the possibility of doing band gap engineering on the nanostructures. In order to determine the composition of Ge\(_{1-x}\)Si\(_x\), we performed extended X-ray absorption fine structure (EXAFS) experiments using synchrotron X-radiation from a wiggler source. These results will be presented elsewhere.

**Growth of metallic nanostructures on silicon**

We give an example of growth of self-assembled nanostructures in metal layers on silicon. Growth of metal layers on semiconductor surfaces has been the subject of extensive studies over the decades \(^ {34}\). Here again, one of the goals is to grow quantum wires and quantum dots \(^ {5}\). Recently, a novel electronic growth mechanism has been developed theoretically for such systems, in which the energy contribution of the quantized electrons confined in the metal overlayer can actually determine the morphology of the growing film, prevailing over the strain energy \(^ {35,36}\). This has generated additional interest in such

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**Figure 4.** RHEED patterns from (a) Si(100) (2 x 1) surface, (b) Ge/Si(100) during growth and (c) Ge/Si(100) after deposition of 1.2 nm Ge.

**Figure 5.** STM image showing MBE-grown, self-assembled Ge nanoislands on Si(100).
metal-on-semiconductor systems. Here, we present some preliminary growth results of Ag on Si(111) surfaces. Ag was deposited on a clean Si(111) surface at a rate of 0.34 nm/min, with the substrate at room temperature. Ag films were then annealed at higher temperatures (600–700°C). The thickness of the deposited films was ~4 nm. The STM image in Figure 7 shows that equilateral-triangular Ag islands of nanometer dimensions have grown. These islands have grown on a thick, large island. The triangular-island growth is a consequence of the threefold symmetry of the Si(111) surface. Earlier, Sekar et al. observed growth of equilateral-triangular gold silicidic islands on Si(111) surfaces. Also, trapezoidal islands were observed. Kinetic Monte Carlo simulation of growth on substrates of threefold symmetry predicts several possible shapes of islands, which include these shapes. It also predicts the growth of hexagonal-shaped islands. We have produced hexagonal-shaped, self-assembled islands by MBE growth of Ag on Si(111). These are shown in the STM image of Figure 8. We have identified two distinct strain states in this nanostructural Ag by X-ray diffraction studies (Goswami, D. K. and Dev, B. N., unpublished data). Scanning tunnelling spectroscopy studies on these islands to explore resonant tunnelling behaviour, due to discrete energy levels in these islands, and single electron tunnelling at low temperature are in progress.

Conclusions

MBE is the most advanced technique for the growth of controlled epitaxial layers. With the advancement of nanoscience and nanotechnology, lower dimensional nanostructures are being fabricated by lithographic techniques from two-dimensional epitaxial layers. Alternately, self-assembled, lower dimensional nanostructures can be fabricated directly by self-assembly during MBE growth. Recently, we have installed a cost-effective, compact, custom-made MBE system in our laboratory. Using this facility, we have grown self-assembled, epitaxial nanostructures of semiconductors and metals on silicon substrates. Some examples have been presented here. We have also presented various during-growth and post-growth characterizations of these structures by RHEED, STM and TEM. It is extremely important to obtain a clean surface of the substrate on which the epilayer deposition is inten...
ded. Preparation and characterizations of clean surfaces have been presented for (111) and (100) surfaces of single crystalline-silicon substrates. As presented through examples, these experimental facilities provide versatility in surface physics and nanostructural research.


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